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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/738,405	YAUNG ET AL
	Examiner	Art Unit
	John B. Vigushin	2841

aa.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-17 and 22-25* is/are allowed.

6)☒ Claim(s) *1-3,5-7,12 and 18-21* is/are rejected.

7)☒ Claim(s) *4,8-11 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1203 & 0405*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities:

In Claim 9, "titled" should be changed to --tilted--.

Appropriate correction is required.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

McKuen (US 6,068,518) Bora et al. (US 4,761,881)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 12 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by McEuen.

As to Claim 1, McEuen discloses, in Figs. 1A,B, 3A,B, 5A,B and 6: a circuit board (daughtercard) 10a for mounting circuit components, comprising: traces of electrically conductive material disposed on at least one side of the circuit board 10a for electrically interconnecting the circuit components mounted on the circuit board 10a (the circuit components that populate circuit board 10a and the electrically conductive material

forming the interconnection traces of circuit board 10a, are not explicitly depicted in the drawings, but are *inherent* in the electrical structure and contents of "daughtercards" which are disclosed in McEuen to be designed for connection to system circuit boards or motherboards in order to provide additional functionality to said system boards or motherboards; i.e., wherein the "main circuit boards or motherboards can be upgraded or enhanced by connecting sophisticated computer modules or daughtercards," as taught in col.1: 44-48); at least one female interlocking element--i.e, channel 13--on at least one edge of circuit board 10a (Figs. 1A,B) for interlocking with a male interlocking element 23 of a circuit board connector 21 (Figs. 3A,B, 5A,B and 6) that connects the circuit board 10a with another circuit board 20--or, with circuit board 10b by way of connector 21 and main board 20 (Fig. 5B).

As to Claim 12, McEuen further discloses the female interlocking element 13 has a shape including a substantially straight portion 17 open at the edge of the circuit board 10a and a substantially rounded portion (comprising portion 18 and the beveled regions on both sides of portion 18) connected to straight portion 17 (Figs. 1B and 2B).

As to Claim 18, McEuen discloses, in Figs. 1A,B, 3A,B, 5A,B and 6: a circuit board (daughtercard) 10a for mounting circuit components, comprising: interconnecting means for electrically interconnecting the circuit components mounted on the circuit board 10a (the circuit components and interconnecting means of circuit board 10a, not explicitly depicted in the drawings, but *inherent* in the electrical structure and contents of "daughtercards" which are disclosed in McEuen to be designed for connection to system circuit boards or motherboards in order to provide additional functionality to said

system boards or motherboards; i.e., wherein the "main circuit boards or motherboards can be upgraded or enhanced by connecting sophisticated computer modules or daughtercards," as taught in col.1: 44-48); female interlocking means (channel 13) for interlocking with male interlocking means 23 of a circuit board connector 21 for mechanically connecting the circuit board with another circuit board 20 (Figs. 3A,B, 5A,B and 6).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2, 3, 5-7 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over McEuen in view of Bora et al.

A) As to Claims 2 and 19:

I. McEuen is silent as to the specific package types of the components populating circuit board 10a.

IIa. Bora et al. discloses a circuit board having through-holes 42 disposed on the circuit board (Figs. 1 and 2) for mounting a variety of through-hole components, such as components 34 and 38, on the circuit board (Figs. 6 and 9), but does not specify the interconnecting means--i.e., the interconnection traces--that electrically interconnect the through-hole components. The various through-hole components perform electronic functions required for the electronic system application.

IIb. Since the circuit board of Bora et al. is being used in an electronic system application to perform a required function, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include through-hole components 34 and 38 whose functionalities are interdependent and required by the electronic system in an application, and therefore further obvious to provide the circuit board with traces routed such that the components 34 and 38 are interconnected in order to electronically communicate with each other and perform those necessary electronic functions required by the system application.

III. Since McEuen and Bora et al. both teach circuit boards with a variety of components thereon for performing an electronic function in an application, then the selection of use of various leaded and pin-grid components whose functions are needed for an application and whose packaging requires through-hole mounting on a circuit

board, as taught by Bora et al, would have been readily recognized as functional electronic components vital to an electronic application in the pertinent art of McEuen.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select and mount components whose functionality is required for an application and whose packaging requires through-hole mounting on the circuit board, as taught by Bora et al., and wherein the functions of the through-hole mounted components are interdependent and are therefore interconnected by traces on the circuit board, as is strongly suggested and obvious from the circuit board assembly of Bora et al.

B) As to Claim 3, McEuen, as modified by Bora et al., not only teaches the interconnected through-hole components, but further teaches that such components include a dual in-line package (DIP) IC 38 (Figs. 6 and 9; col.2: 47-49).

C) As to Claims 5 and 20:

I. McEuen is silent as to the specific package types of the components populating circuit board 10a.

II. Bora et al. discloses a circuit board having at least one surface-mount means--i.e., surface-mount pads 16, 18--on one side of the circuit board for mounting a variety of surface-mount circuit components 40, 41 on the circuit board (Figs. 1, 2 and 6; col.2: 49-52).

III. Since McEuen and Bora et al. both teach circuit boards with a variety of components thereon for performing an electronic function in an application, then the selection of various surface-mount components whose functions are needed for an

application and whose packaging is designed for surface-mounting on surface-mount pads of a circuit board, as taught by Bora et al, would have been readily recognized as functional electronic components vital to an electronic application in the pertinent art of McEuen.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select and mount components whose functionality is required for an application and whose packaging is designed for surface-mounting on surface-mount pads of the circuit board, as taught by Bora et al.

D) As to Claim 6:

I. McEuen, as modified by Bora et al., discloses that surface-mount circuit components populate the circuit board 10a.

II. Bora et al. further discloses that the surface-mount components include an SO package IC 41 and PLCC package IC 40 (Fig. 6; col.3: 18-21).

III. Since McEuen, as modified by Bora et al., teaches a circuit board with a variety of components thereon for performing an electronic function in an application, then the use of particular IC packages, such as a PLCC or SO package surface-mount component for meeting the functional and packaging specifications of an electronic system, as taught by Bora et al., would have been readily recognized in the pertinent art of McEuen.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to mount any off-the-shelf surface-mount components, such as an SO package IC and/or a PLCC package IC, on the circuit board of McEuen

in order to perform the electronic functions required by the electronic system for an application, as taught by Bora et al.

E) As to Claims 7 and 21:

I. McEuen is silent as to the specific package types of the components populating circuit board 10a.

IIa. Bora et al. discloses a circuit board having at least one surface-mount means (i.e., surface-mount pads 16, 18) on one side of the circuit board for mounting a variety of surface-mount circuit components 40, 41 on the circuit board (Figs. 1, 2 and 6; col.2: 49-52). Bora et al. also discloses that the circuit board additionally has through-hole means--i.e., through-holes 42--disposed thereon (Figs. 1 and 2) for mounting a variety of through-hole components, such as components 34 and 38, on the circuit board (Figs. 6 and 9), but does not specify the interconnection traces that electrically interconnect the components. The various surface-mount and through-hole components perform electronic functions required for the electronic system application.

IIb. Since the circuit board of Bora et al. is being used in an electronic system application to perform a required function, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include through-hole components 34, 38 and surface-mount components 40, 41 whose functionalities are interdependent with one another and required by the electronic system in an application, and therefore further obvious to provide the circuit board with traces routed such that the through-hole components 34, 38 and surface-mount components 40, 41 are interconnected in order

to electronically communicate with each other and perform those necessary electronic functions required by the system application.

III. Since McEuen and Bora et al. both teach circuit boards with a variety of components thereon for performing an electronic function in an application, then the selection of various surface-mounted and through-hole mounted components whose functions are needed for an application and whose packaging is designed for surface-mounting or through-hole mounting on surface-mount pads or through-holes of a circuit board, as taught by Bora et al, would have been readily recognized as functional electronic components vital to an electronic application in the pertinent art of McEuen.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select and mount components whose functionality is required for an application and whose packaging is designed for surface-mounting on surface-mount pads of the circuit board or through-hole mounting on the circuit board, as taught by Bora et al., and wherein the functions of the surface-mount and through-hole mounted components are interdependent and are therefore interconnected by traces on the circuit board, as is strongly suggested and obvious from the circuit board assembly of Bora et al.

Allowable Subject Matter

8. Claims 14-17 and 22-25 have been allowed.

9. Claims 4, 8-11 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

Claims 4 and 8-11 state the allowable subject matter in their respective entirety.

In Claims 13, 22-24 and 25 patentability resides in *the male interlocking element having a first half part inserted into the female interlocking element of a first circuit board and a second half part inserted into the female interlocking element of a second circuit board*, in combination with the other limitations of Claim 13 and base Claims 22 and 25, respectively.

11. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Lin (US 5,014,163) discloses a circuit board connector having two or more **female** interlocking elements 21, 31, 41, or 44 (Figs. 3, 4 and 5), thus forming half or quarter female connectors for receiving the **male** interlocking elements 11 (Fig. 2) of the circuit boards (e.g., Figs. 6, 6-2 and 7). Applicant's claims require that the circuit board

connector have the *male* interlocking elements while the circuit boards have the *female* interlocking elements.

b) Dorinski et al. (US 5,110,298) discloses circuit boards configured with male interlocking elements 102 and female interlocking elements 104 (Figs. 1 and 2) for joining the circuit boards to form a larger circuit board (Figs. 3, 4 and 5), wherein the interlocking elements form a friction or interference fit, thus obviating a solder connection (col.2: 55-62).

c) Bauermeister (US 2002/0080590 A1) discloses circuit boards configured with male interlocking elements 4 and female interlocking elements 5 for joining the circuit boards 7 and 7', the male and female interlocking elements 4 and 5 captively engaging to form a larger circuit board. wherein the interlocking connection is reinforced by solder (Fig. 1; paragraphs [0019] and [0020]).

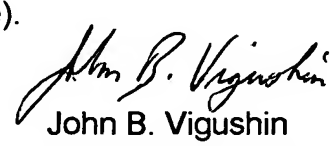
d) Rank (US 4,523,796) discloses a circuit board connector 22 with a first half part for receiving a first circuit board 12 and a second half part for receiving a second circuit board 14 but teaches a spring force, alternatively used in conjunction with strips of adhesive tape, for contact retention of the circuit boards 12, 14 with the connector 22 (Figs. 1 and 2; col.5: 45-57); not interlocking elements.

e) *Khoury (US 6,369,445 B1)* discloses chip carriers 100 interconnected by means of male and female interlocking elements on the edges 106, 108 of the carriers 100 (col.3: 52-67) and further teaches that the carrier 100 could be made of semiconductor or insulating materials [see col.3: 52-55 in conjunction with *Khoury (US 6,343,940 B1*: Fig. 6A and col.6: 65-col.7: 4].

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
December 25, 2005